

What is claimed is:

1. A switch circuit comprising:
 - an input terminal which receives an input signal;
 - 5 an internal circuit which executes a predetermined function;
 - a first switch element which is coupled between the input terminal and the internal circuit and which has a control gate receiving a control signal, a first electrode coupled to the input terminal, and a second electrode; and
 - a second switch element which is coupled between the input terminal and
 - 10 the internal circuit and which has a control gate receiving the control signal, a first electrode coupled to the second electrode of the first switch element, and a second electrode coupled to the internal circuit.
2. The switch circuit according to Claim 1, wherein the first switch
- 15 element comprises a first MOS transistor of an n-type and the second switch element comprises a second MOS transistor of a p-type
3. The switch circuit according to Claim 2, wherein the second MOS
- transistor has a substrate terminal connected to the second electrode of the second
- 20 MOS transistor.
4. The switch circuit according to Claim 1, wherein the first switch
- element comprises a first MOS transistor of a p-type and the second switch
- element comprises a second MOS transistor of an n-type.
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5. The switch circuit according to Claim 4, wherein the first MOS
- transistor has a substrate terminal connected to the second electrode of the first

MOS transistor.

6. The switch circuit according to Claim 1, further comprising:
another internal circuit which executes a predetermined function; and
5 a third switch element which is coupled between the input terminal and
another internal circuit and which has a control gate receiving the control signal, a
first electrode coupled to the input terminal, and a second electrode coupled to
another internal circuit.
- 10 7. The switch circuit according to Claim 6, wherein the internal circuit is
an analog circuit and another internal circuit is a digital circuit.